

IEEE HOME | SEARCH IEEE | SHOP | WEB ACCOUNT | CONTACT IEEE

Membership Publications/Services Standards Conferences Careers/Jobs

IEEE Xplore®
RELEASE 1.4Welcome
United States Patent and Trademark Of[Help](#)
[Review](#)[FAQ](#)[Terms](#)[IEEE Peer](#)[Quick Links](#)» [Sea](#)**Welcome to IEEE Xplore®**

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

[Print Format](#)Your search matched **19** of **942182** documents.

A maximum of **19** results are displayed, **25** to a page, sorted by **Relevance** in **descending** order.
 You may refine your search by editing the current search expression or entering a new one the text b
 Then click **Search Again**.

(joshi or kroell) and soi

[Search Again](#)**Results:**Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD****1 Effects of gate-to-body tunneling current on PD/SOI CMOS SRAM**

Joshi, R.V.; Chuang, C.T.; Fung, S.K.H.; Assaderaghi, F.; Sherony, M.; Yang, I Shahidi, G.;

VLSI Technology, 2001. Digest of Technical Papers. 2001 Symposium on , 2001
 Page(s): 75 -76

[\[Abstract\]](#) [\[PDF Full-Text \(184 KB\)\]](#) **IEEE CNF****2 Design considerations of scaled sub-0.1 μm PD/SOI CMOS cir**

Chuang, C.T.; Joshi, R.V.; Kim, K.;

Quality Electronic Design, 2003. Proceedings. Fourth International Symposium
 2003

Page(s): 153 -158

[\[Abstract\]](#) [\[PDF Full-Text \(3578 KB\)\]](#) **IEEE CNF****3 A 660 MHz self-resetting 8 port, 32x64 bits register file and latch in 0 μm SOI technology**

Joshi, R.V.; Hwang, W.; Henkels, W.H.; Wilson, S.; Rausch, W.; Shahidi, G.;

SOI Conference, 1998. Proceedings., 1998 IEEE International , 5-8 Oct 1998

Page(s): 131 -132

[\[Abstract\]](#) [\[PDF Full-Text \(228 KB\)\]](#) **IEEE CNF****4 Detailed analysis of the gate delay variability in partially depleted SO circuits**

Aller, I.; Kroell, K.E.;

SOI Conference, 1999. Proceedings. 1999 IEEE International , 1999

Page(s): 40 -41

[\[Abstract\]](#) [\[PDF Full-Text \(112 KB\)\]](#) **IEEE CNF**

5 Frequency dependent behavior of a high performance dynamic register in 1.8 V, 0.25 μm SOI technology

Joshi, R.V.; Hwang, W.; Wilson, S.C.; Shahidi, G.; Chuang, C.T.;
SOI Conference, 1999. Proceedings. 1999 IEEE International , 1999
Page(s): 79 -81

[\[Abstract\]](#) [\[PDF Full-Text \(132 KB\)\]](#) **IEEE CNF**

6 Novel 3-D structures [ICs]

Saraswat, K.C.; Souri, S.J.; Subramanian, V.; Joshi, A.R.; Wang, A.W.;
SOI Conference, 1999. Proceedings. 1999 IEEE International , 1999
Page(s): 54 -55

[\[Abstract\]](#) [\[PDF Full-Text \(108 KB\)\]](#) **IEEE CNF**

7 Implementation of a high speed multiport register file in a 1.8 V, 0.25 μm CMOS bulk and SOI technology

Joshi, R.V.; Hwang, W.; Wilson, S.; Shahidi, G.; Chuang, C.T.;
VLSI Technology, Systems, and Applications, 1999. International Symposium o
1999
Page(s): 274 -277

[\[Abstract\]](#) [\[PDF Full-Text \(236 KB\)\]](#) **IEEE CNF**

8 Design considerations and implementations of a high performance dy register file

Joshi, R.V.; Hwang, W.;
VLSI Design, 1999. Proceedings. Twelfth International Conference On , 7-10 Ja
Page(s): 526 -531

[\[Abstract\]](#) [\[PDF Full-Text \(984 KB\)\]](#) **IEEE CNF**

9 A low power 900 MHz register file (8 ports, 32 words \times 64 bits) in 1.8 μm SOI technology

Joshi, R.V.; Hwang, W.; Wilson, S.; Shahidi, G.; Chuang, C.T.;
VLSI Design, 2000. Thirteenth International Conference on , 2000
Page(s): 44 -49

[\[Abstract\]](#) [\[PDF Full-Text \(728 KB\)\]](#) **IEEE CNF**

10 Controlling floating-body effects for 0.13 μm and 0.10 μm SO CMOS

Fung, S.K.H.; Zamdmer, N.; Oldiges, P.J.; Sleight, J.; Mocuta, A.; Sherony, M. S.-H.; Joshi, R.; Chuang, C.T.; Yang, I.; Crowder, S.; Chen, T.C.; Assaderaghi, Shahidi, G.;

Electron Devices Meeting, 2000. IEDM Technical Digest. International , 2000
Page(s): 231 -234

[\[Abstract\]](#) [\[PDF Full-Text \(380 KB\)\]](#) **IEEE CNF**

11 High frequency input isolation circuit for asynchronous CMOS macro PD/SOI technology

Joshi, R.V.; Hwang, W.; Chuang, C.T.;

SOI Conference, 2000 IEEE International , 2000
Page(s): 140 -141

[\[Abstract\]](#) [\[PDF Full-Text \(116 KB\)\]](#) **IEEE CNF**

12 "Cool low power" 1 GHz multi-port register file and dy latch in 1.8 V, 0.25 μm SOI and bulk technology

Joshi, R.V.; Hwang, W.; Wilson, S.C.; Chuang, C.T.;

Low Power Electronics and Design, 2000. ISLPED '00. Proceedings of the 2000 International Symposium on , 2000
Page(s): 203 -206

[\[Abstract\]](#) [\[PDF Full-Text \(296 KB\)\]](#) **IEEE CNF**

13 Electrothermal modeling of ESD diodes in bulk-Si and SOI technolog

Yu Wang; Juliano, P.; Joshi, S.; Rosenbaum, E.;

Electrical Overstress/Electrostatic Discharge Symposium Proceedings 2000 , 20
Page(s): 430 -436

[\[Abstract\]](#) [\[PDF Full-Text \(404 KB\)\]](#) **IEEE CNF**

14 Novel circuits to improve SRAM performance in PD/SOI technology

Joshi, R.V.; Bhavnagarwala, A.; Hsu, L.L.; Chuang, C.T.; Hwang, W.;

SOI Conference, 2001 IEEE International , 2001
Page(s): 99 -100

[\[Abstract\]](#) [\[PDF Full-Text \(200 KB\)\]](#) **IEEE CNF**

15 SOI-optimized 64-bit high-speed CMOS adder design

Jae-Joon Kim; Joshi, R.; Ching-Te Chuang; Roy, K.;

VLSI Circuits Digest of Technical Papers, 2002. Symposium on , 2002

Page(s): 122 -125

[\[Abstract\]](#) [\[PDF Full-Text \(364 KB\)\]](#) **IEEE CNF**

16 High performance SRAMs in 1.5 V, 0.18 μ m partially depleted technology

Joshi, R.V.; Pellela, A.; Wagner, O.; Chan, Y.H.; Dachtera, W.; Wilson, S.; Kow S.P.;

VLSI Circuits Digest of Technical Papers, 2002. Symposium on , 2002

Page(s): 74 -77

[\[Abstract\]](#) [\[PDF Full-Text \(359 KB\)\]](#) **IEEE CNF**

17 Performance assessment of scaled strained-Si channel-on-insulator CMOS

Keunwoo Kim; Ching-Te Chuang; Rim, K.; Joshi, R.V.;

SOI Conference, IEEE International 2002 , 7-10 Oct 2002

Page(s): 17 -19

[\[Abstract\]](#) [\[PDF Full-Text \(281 KB\)\]](#) **IEEE CNF**

18 Thermal conductivity model for thin silicon-on-insulator layers at high temperatures

Asheghi, M.; Behkam, B.; Yazdani, K.; Joshi, R.; Goodson, K.E.;

SOI Conference, IEEE International 2002 , 7-10 Oct 2002

Page(s): 51 -52

[\[Abstract\]](#) [\[PDF Full-Text \(246 KB\)\]](#) **IEEE CNF**

19 High performance low power V_{DD} -wave-pipeline CMOS circuit in PD/SOI technology

Joshi, R.V.; Yee, F.; Kim, K.; Williams, R.Q.; Chuang, C.T.;

SOI Conference, IEEE International 2002 , 7-10 Oct 2002

Page(s): 128 -129

[\[Abstract\]](#) [\[PDF Full-Text \(251 KB\)\]](#) **IEEE CNF**

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) | [Advanced Search](#)
[Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedback](#) | [Technical Support](#) | [Email Alerting](#)
[No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#) | [FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2003 IEEE — All rights reserved